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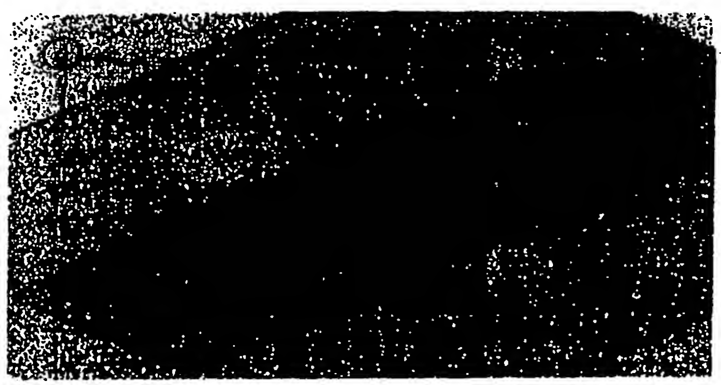
(54) Title: INTEGRATED GAS FLOW SENSOR BASED ON POROUS SILICON MICROMACHINING

(57) Abstract

The device of the integrated gas flow sensor is fabricated on a membrane made of a bilayer of SiO_2/polysilicon on bulk crystalline silicon. The membrane is either suspended on a deep cavity formed on bulk crystalline silicon, or it is lying on a thick oxidized porous silicon layer. The cavity under the membrane is fabricated by bulk silicon micromachining using porous silicon as a sacrificial layer. The sensing element is composed of a two series of integrated thermocouples on the left and right side of a heated resistor. The thermocouples are composed of parallel strips of aluminum/p-type polysilicon or p-type/n-type polysilicon, in contact on one end. The heated resistor is a p-type polysilicon strip. A second polysilicon resistor outside the membrane in series with the heated resistor serves to stabilize the heating power to better than 0.05 %. The fabrication process is C-MOS compatible and the sensor is easily integrated on silicon with its readout electronics.



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Title: "Integrated gas flow sensor based on porous silicon micromachining"

Technical field

The device is an integrated gas flow sensor which uses a series of integrated thermocouples, the hot contact of which is on a polycrystalline silicon membrane and the cold contact on bulk silicon. The membrane is either suspended on a deep cavity formed into silicon by using porous silicon as a sacrificial layer or as an alternative the porous silicon is not removed but oxidized and it is used as thermal isolation layer. A heated resistor is also integrated on the membrane. Integrated thermopiles measure gas flow through Seebeck effect. The polysilicon thermally isolated resistor is heated with constant power and the temperature is measured by the thermopiles. A gas flow changes the resistor temperature and therefor the output voltage of the thermopile. We can also use the flow-dependent heat transport from the heater into the surrounding gas. The gas flow generates a temperature difference between downstream and upstream points on the device, which provides different thermopile signals.

Technical level of existing technology

Existing integrated gas flow sensors on silicon use in general a heated resistor and the temperature difference due to the gas flow is measured by a transistor pair or a resistance bridge (examples are : The European patent No 0490764A1, the US patent No 4,680,963 and the US patent No 5,231,878).). The use of integrated thermocouples increases the sensitivity of the device, which is controlled by the number of the thermocouples. Thermopiles have also various attractive properties compared with the above mentioned sensors. First, the thermopile is based on the self-generating Seebeck effect, in which the input signal supplies the power for the output signal. This ensures that the thermopile has an output signal without offset drift, because there cannot be any output signal without input power. Second, the thermopile does not suffer from interference from any physical or chemical signals except light (which can easily be shielded) because the Seebeck effect and the photoelectric effect are the only two self-generating effects in silicon. Third, the thermopile does not need any biasing. The read-out is very simple and only a voltmeter is required. Finally there is no interference caused by power supplies. The

other advantage is that a process which is C-MOS compatible is used. The sensor is so compatible with the existing silicon technology and may be integrated with the control circuit on the same substrate.

Description

The device is an integrated gas flow sensor composed of integrated thermocouples on a polycrystalline silicon membrane, suspended on a cavity on bulk crystalline silicon, used as substrate. The insulating layer between the membrane and the thermocouples is silicon dioxide or silicon nitride. A heated resistor is also integrated on the membrane [1]. In fig. 1 we can see : the silicon substrate (2), the polysilicon / SiO_2 membrane and the isolation (3), the polysilicon part of thermopiles (4), the aluminum part of thermopiles (5) and the cavity after porous silicon removal (6). The cavity under the membrane is formed by using bulk silicon micromachining. To this end, a porous silicon layer is formed locally on silicon by electrochemical dissolution of bulk crystalline silicon and it is then chemically removed by C-MOS compatible chemicals ($HF:H_2O_2$) in order to form the cavity. Before porous silicon removal, a bilayer consisting of the thermal isolation layer and polycrystalline silicon is deposited on top of the whole silicon area and it is etched selectively in order to define the membrane area. The cavity under the membrane may be as deep as several tens of μms [2]. Fig. 2 shows a top view (A) and a cross section (B) of the membrane, where we can see the monocrystalline silicon (1) and the membrane (2). The thermal isolation may also be obtained by a porous silicon oxide layer, so an alternative to the above process is to keep porous silicon in place and oxidize it.

The integrated thermocouples on the membrane are put in series and their number determines the sensitivity of the device. These thermocouples are in thin film form (parallel strips of Al/n-type polysilicon or p-type/n-type polysilicon) and they are connected together in series so as a total voltage difference is measured at the two ends of the thermocouple series. The measured voltage difference is due to a temperature difference, developed at the two ends of each thermocouple, due to Seebeck effect, when there is a temperature difference caused by the gas flow.

The whole process is C-MOS compatible and the main steps are described in fig.3 where we can see : the definition of porous silicon area (A), the definition of membrane area and lateral isolation (B), the first step in thermopile fabrication (C) and finally the second step of thermopile

fabrication and porous etching. The main parts of the device are : porous silicon (1), silicon substrate (2), polysilicon / SiO_2 membrane and isolation (3), polysilicon strips - thermopiles (4), aluminum strips - thermopiles and puds (5) and cavity after porous silicon removal (6).

Claims

We claim :

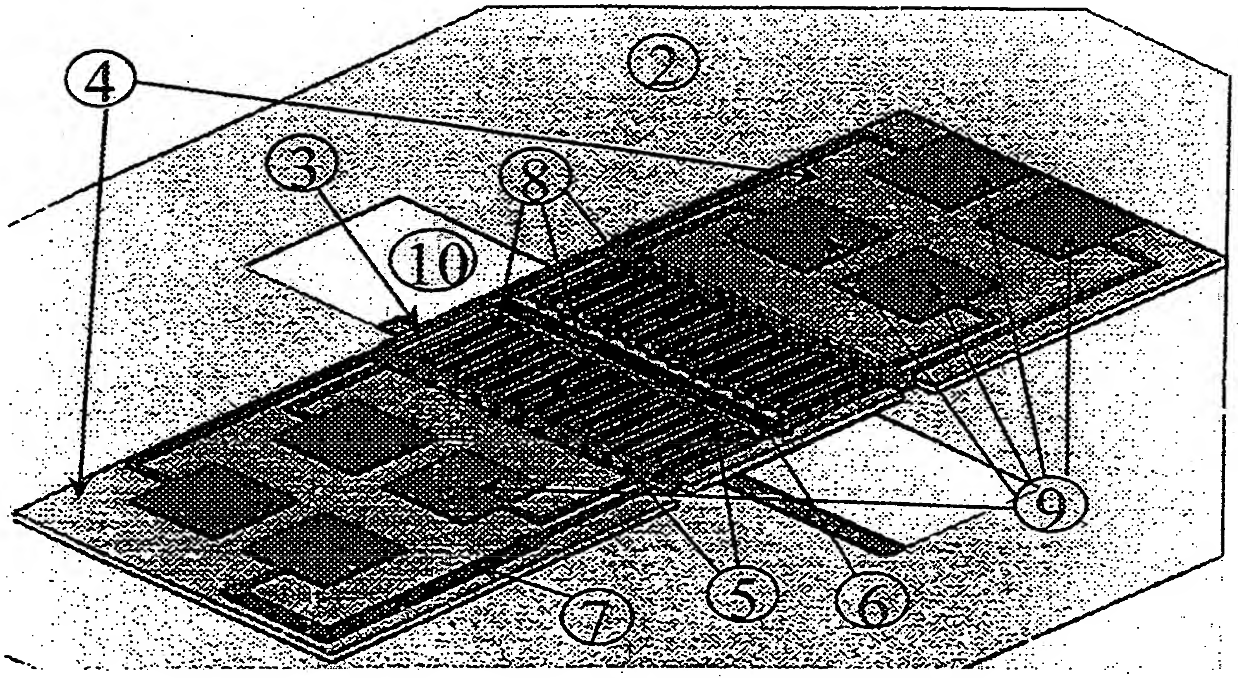
1. An integrated gas flow sensor device characterized by : a sensing element composed of a series of integrated thermocouples(5,8) and a heated resistor(6) both integrated on a suspended membrane(3) composed of a bilayer of polysilicon/SiO_2 or polysilicon/silicon nitride. The membrane is suspended on a deep tunnel(10), formed into a monocrystalline silicon substrate(2). The deep tunnel(10) under the membrane(3) serves to thermally isolate the sensor from the silicon substrate(2). It is formed by bulk silicon micromachining, using a porous silicon layer(1) as sacrificial layer. The thermocouples are parallel strips in contact on one end, made of p-type polycrystalline silicon(5) / aluminum(5) or n-type / p-type polycrystalline silicon. The resistor(6) is also a strip made of polycrystalline silicon.

2. The fabrication process of a gas flow sensor as described in claim 1, characterized by C-MOS compatibility. All the processes and chemicals used are C-MOS compatible. A porous silicon layer(1) is formed on a pre-defined area by electrochemical dissolution of bulk crystalline silicon(2). A bilayer of silicon dioxide and polycrystalline silicon(3) is then deposited on top by Low Pressure Chemical Vapour Deposition and etched by Reactive Ion Etching, in order to define the membrane area(3) and the pads(4). The thermopiles(5,8), the heater resistor(6), the stabilizer resistor(7) and the contact pads(9) are formed on the membrane(3) and on the pads(4) by first depositing polysilicon which is doped with p-type dopants and etched selectively by Reactive Ion Etching and then by depositing aluminum, which is etched chemically. At the end of the process, the porous silicon layer(1) is removed by C-MOS compatible chemicals ($HF:H_2O_2$) and a deep tunnel(10) is thus formed under the membrane(3), which thermally isolates the sensor from the bulk silicon substrate(2).

3. An alternative process to the fabrication process of claim 2, in which the thermal isolation between the membrane(3) and the bulk silicon(2) substrate is assured by the porous silicon layer which is thermally oxidized in order to achieve better thermal isolation properties. The thermal conductivity of oxidized porous silicon is between two and three orders of magnitude lower than the thermal conductivity of monocrystalline silicon. So it provides thermal isolation close to that obtained by air which has a thermal conductivity four orders of magnitude below that of silicon.

4. Suspended membrane(3) fabrication process which is based on bulk silicon micromachining and it is characterized by C-MOS compatibility as it is described in claim 2. The deep cavity(10) under the membrane may be as

deep as several tens of μms and it is fabricated by using porous silicon(1) as a sacrificial layer. A porous silicon layer(1), of a thickness of several micrometers to several tens of micrometers is fabricated locally on a predefined area by electrochemical dissolution of bulk crystalline silicon(2) through a mask made of a bilayer of SiO_2 and polycrystalline silicon. The membrane material(3) is then deposited on top of the whole wafer by Low Pressure Chemical Vapour Deposition and it is etched by Reactive Ion Etching in order to define the membrane area(3). The porous silicon(11) is then chemically removed by a solution of $HF{:}H_2O_2$ which is C-MOS compatible. A polysilicon bridge(3) is so formed with a deep tunnel(10) underneath. The bottom surface and sidewalls of the tunnel are very smooth.



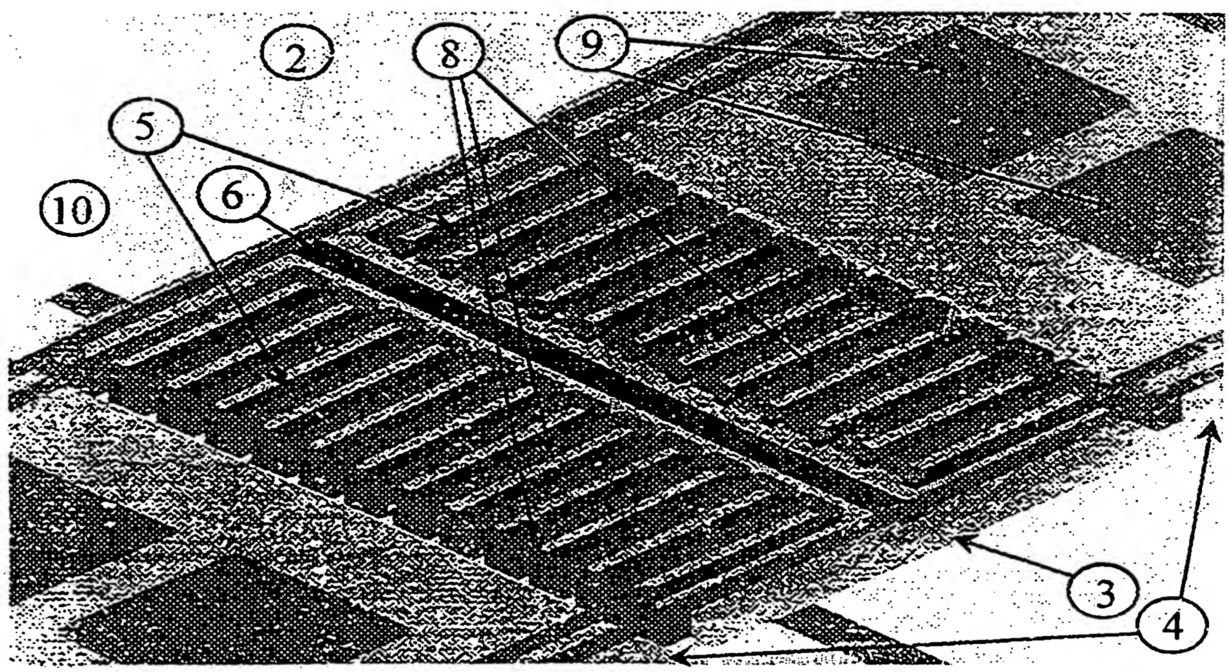


Fig. 1/3

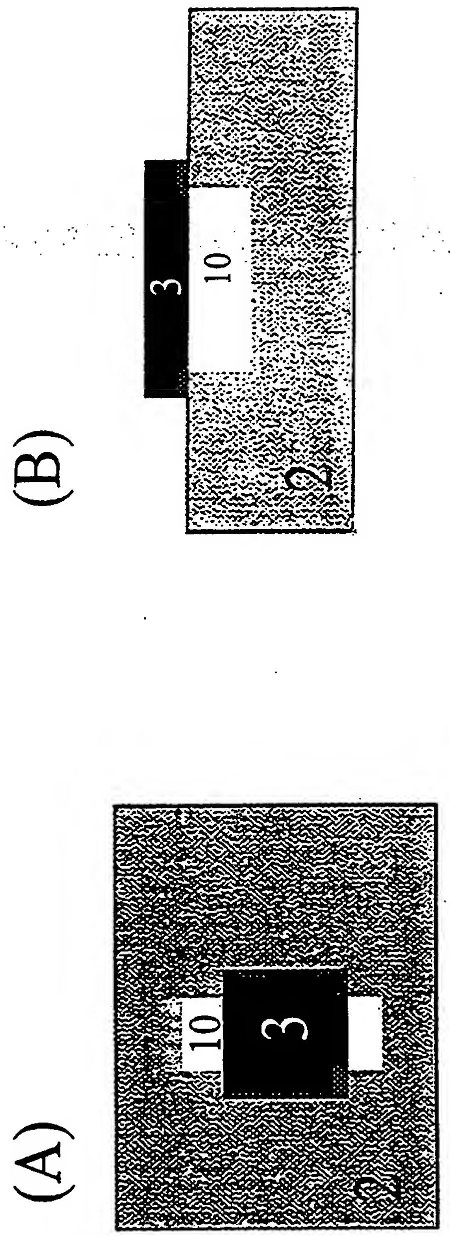


Fig. 2/3

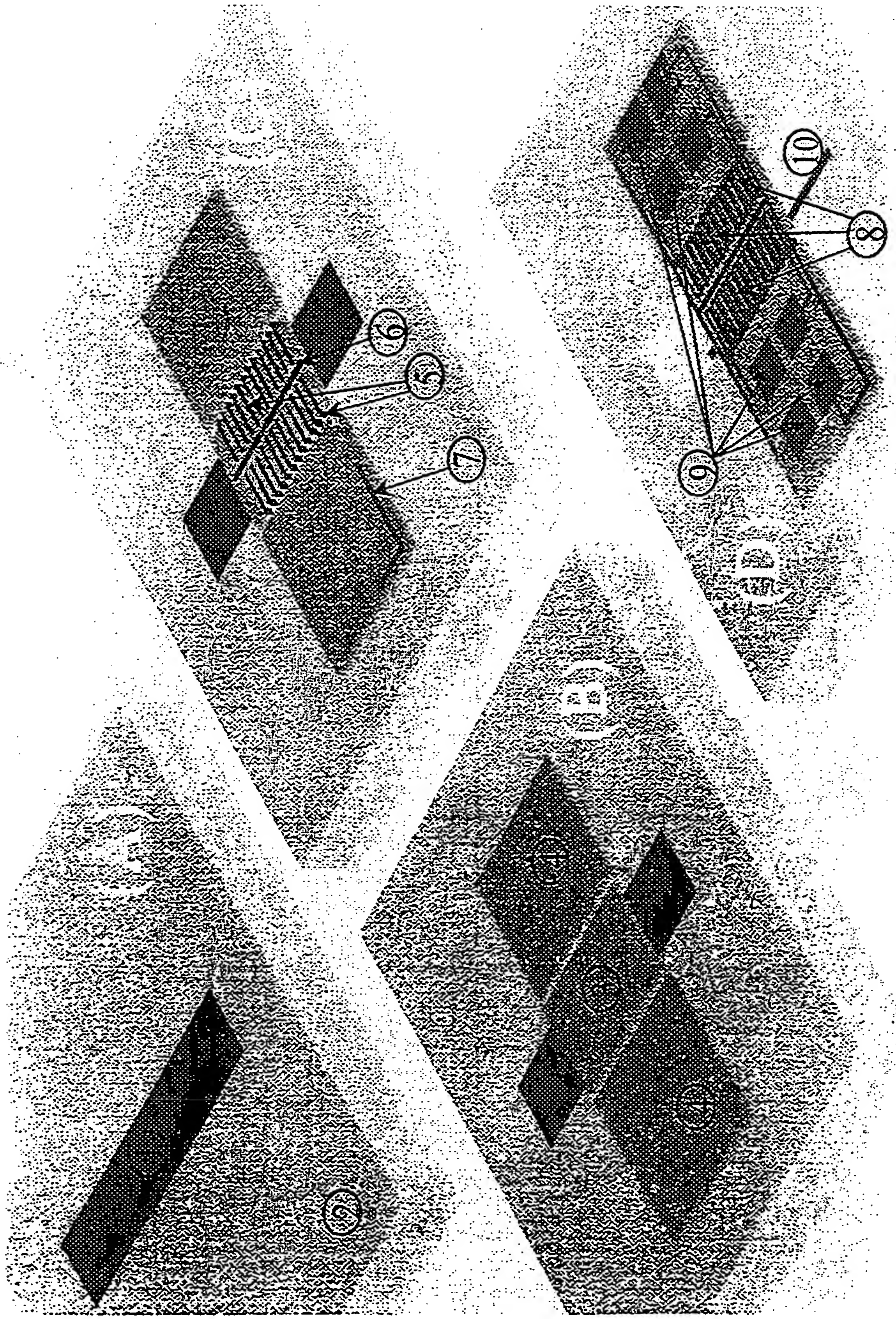


Fig. 3/3

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/GR 97/00040

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01F1/684 G01F1/688

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01F G01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 195 20 777 C (INST PHYSIKALISCHE HOCHTECHNOL) 29 August 1996 see the whole document ---	1-4
A	DE 43 03 423 A (FRAUNHOFER GES FORSCHUNG) 11 August 1994 see column 2, line 44 - column 3, line 10; figures ---	1-4
A	DE 44 18 207 C (SIEMENS AG) 22 June 1995 see page 3, line 15 - line 60; figures ---	1-4
A	GB 2 251 312 A (BOSCH GMBH ROBERT) 1 July 1992 see the whole document --- -/--	1-4

[X] Further documents are listed in the continuation of box C.

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Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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